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## ABSTRACT OF THE DISCLOSURE

An SRAM memory cell having first and second transfer gate transistors. The first transfer gate transistor includes a first source/drain connected to a bit line and the second transfer gate transistor has a first source/drain connected to a complement bit line. Each transfer gate transistor has a gate connected to a word line. The SRAM memory cell also includes first and second pull-down transistors configured as a storage latch. The first pull-down transistor has a first source/drain connected to a second source/drain of said first transfer gate transistor; the second pull-down transistor has a first source/drain connected to a second source/drain of said second transfer gate transistor. Both first and second pull-down transistors have a second source/drain connected to a power supply voltage node. The first and second transfer gate transistors each include a gate oxide layer having a first thickness, and the first and second pull-down transistors each include a gate oxide layer having a second thickness, wherein and the first thickness is different from the second thickness.